WHAT IS CLAIMED IS:

1. A data recovery system, comprising:

first and second data sampling elements;

a clock interpolator to receive a first differential clock and output a second differential clock, said first differential clock operating the first data sampling element, and said second differential clock operating the second data sampling element;

a data interpolator to receive and output differential data signals, said received differential data signal being sampled by the first data sampling element, and said output differential data signal being sampled by the second data sampling element; and

a mechanism to steer current between first and second nodes, the first node being coupled to bias an input differential pair of the clock interpolator and a delayed differential pair of the data interpolator, and the second node being coupled to bias an input differential pair of the data interpolator and a delayed differential pair of the clock interpolator.

2. The data recovery system of claim 1, wherein the mechanism to steer current is configured to steer more current to the second node.

3. The data recovery system of claim 1, wherein matched delays between the input and delayed differential pairs are implemented via

additional differential pairs.

4. The data recovery system of claim 1, wherein matched delays between the input and delayed differential pairs are implemented via matched traces.

5. The data recovery system of claim 1, wherein matched delays between the input and delayed differential pairs are less than a rise time of the received differential data signal.

6. The data recovery system of claim 1, wherein the current steering mechanism is programmable to steer different ratios of currents to the first and second nodes.

7. A method for providing an oversampling delay between clock and data signals, comprising:

steering a current between first and second nodes, said first node being coupled to an input differential pair of a clock interpolator and a delayed differential pair of a data interpolator, and said second node being coupled to an input differential pair of the data interpolator and a delayed differential pair of the clock interpolator;

providing first clock and data signals to a first data sampling element and, respectively, to said clock and data interpolators; and

providing second clock and data signals, respectively output from the clock and data interpolators, to a second data sampling element.

8. The method of claim 7, further comprising:

providing the second clock and data signals to inputs of a chain of N more clock and data interpolators; and

providing clock and data outputs of the chain of clock and data interpolators to N additional data sampling elements.

9. The method of claim 7, further comprising, steering more current to the second node.

10. The method of claim 7, further comprising, steering different ratios of currents to said first and second nodes to determine a useful oversampling period.